

Design Example Using the altlvds Megafunction & the External PLL Option in Stratix II Devices

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Application Note 409

Introduction	The altlvds megafunction allows you to instantiate an external phase-locked loop (PLL) when using Stratix [®] II, HardCopy [®] II, or Cyclone [™] II devices. This external PLL is a fast PLL set-up in LVDS mode. This option gives you more control over the PLL settings, and gives you access to PLL options such as bandwidth and dynamic reconfiguration, which are unavailable when instantiating the serializer/deserializer (SERDES) circuitry using the altlvds megafunction.	
	If you are not using the specialized PLL features, the external PLL option provides no benefit and should not be used with the altlvds megafunction.	
Quartus II Project	The project discussed in this application note contains a complete design illustrating the connections between the external fast PLL and the altlvds receive megafunctions. A complete ModelSim [®] project, including simulation files demonstrating the functionality of the design, is available on the Altera [®] website.	
	Download the Design Files	
	The design files for this example are available on the Altera website, on both the literature page and the PLL & Clocking Design Examples page located at http://www.altera.com/support/examples/functionality/pll-clocking.html.	
	The example in these design files uses the LVDS receiver in the external PLL mode.	
	Example	
	The following example uses the MegaWizard [®] Plug-In Manager in the Quartus [®] II software to generate the altpll and altlvds megafunctions.	

In this example, you will perform the following activities:

- Generate a high-speed differential receiver using the altlvds megafunction and the MegaWizard Plug-In Manager
- Generate the PLL using the MegaWizard Plug-In Manager
- Simulate the high-speed differential interface design using ModelSim

Design Details

This design consists of two megafunctions, altpl1 and altlvds. The function of this design is to convert four serial input channels into a 32-bit wide output bus with a deserialization factor of eight. The idea of this design is to show how to use the altlvds megafunction with an external PLL, as well as the altpl1 and the altlvds megafunction settings necessary for the correct operation. Refer to Table 1 for design specifications.

Table 1. Design Specifications						
Specification	Inputs	Outputs	Details			
altlvds	<pre>rx_datain[4:0], data rate 800 Mb/s</pre>	rx_out[31:0]	No built-in PLL			
altpll	tx_inclock = 100 MHz	<pre>c0 = 100 MHz, // Core Clock sclkout0 = 800 MHz = data rate enable0 = enable pulse</pre>	The enable pulse is generated once in 10 ns because the enable pulse period corresponds to the bigger of the two clock periods of core clock and sclkout0.(1)			

Note to Table 1:

(1) sclkout0 is at a -180 degree phase shift to the VCO clock.

PLL inputs and outputs are shown in Figure 1.





Generate an altlvds Receiver

This section describes how to generate the altlvds and altpll megafunctions to generate an altlvds receiver using the MegaWizard Plug-In Manager.

- 1. Start the Quartus II software. On the Tools menu, click **MegaWizard Plug-In Manager**. Page 1 is shown.
- 2. Select **Create a new custom megafunction variation**, and click **Next**. Page 2a is shown.
- 3. On page 2a, in the Installed Plug-Ins list under I/O, select ALTLVDS. In the Which device family will you be using? list, select Stratix II. In the What name do you want for the output file? field, type the name of the output file. Select the output file type. Click Next. Page 3 is shown (Figure 2).

Figure 2. MegaWizard Plug-in Manager—ALTLVDS, Page 3

MegaWizard Plug-In Manager - ALTLVDS [page 3 of 20]				
ALTLVDS Version 6.0	About Documentation			
Parameter Settings General Receiver settings				
attivds.v	Currently selected gevice family: Stratix II			
/rx_inclock LVDS Receiver /rx_enable 4 channels, x8	This module acts as an C LVDS transmitter C LVDS transmitter			
rx_channel_data_align(3.0)	Implement Serializer/Deserializer circuitry in logic cells The receiver starts capturing the LVOS stream at the first fast clock edge. This is intended for solw speeds and byte alignment may be different from the hard SERDES implementation.			
Strati	Enable Dynamic Phase Alignment mode (receiver only) What is the number of ghannels? 4			
Personana librar	What is the descrialization factor?			
4 stratixii_lvds_receiver	Cancel < Back Next > Einish			

- 4. In the Currently selected device family list, select Stratix II.
- 5. Under This module acts as an, select LVDS receiver.
- 6. Turn on Use External PLL. This option is necessary if you want to take advantage of the Stratix II fast PLL features not accessible through the altlvds wizard. When you turn on this option, a warning dialog box is shown (Figure 3).



This warning dialog box displays a list of requirements necessary to take advantage of the Stratix II fast PLL features. Selecting not to register the outputs of the receiver requires the following:

a. The clock and enable from the PLL feed the receiver—the output pins sclkout0 and enable0 of the PLL drive the input pins rx_inclock and rx_enable of the altlvds megafunction (Figure 4).

Figure 4. Connection Between altpll & altivds



b. The outputs are registered in the logic fed by the receiver—the outputs must be pre-registered in the logic fed by the receiver in the connection between altpll and altlvds. Figure 5 shows the synchronization registers (rx_sync_reg) added at the receiver output.



c. A 'Source Multicycle' assignment with a value of DESERIALIZATION_FACTOR should be specified from the receiver atom(s) to the output registers—specify a source multicycle assignment with a value of DESERIALIZATION_FACTOR from the receiver atoms (rx_out) to the output registers (rx_sync_reg).

Without the multicycle assignment, the Quartus II timing analyzer performs the timing analysis with overly conservative numbers, as the data is transferred from the high-speed transmitter clock to slow-speed synchronization registers.

The rx_out data is clocked by the fast clock sclkout0 at 800 MHz, or with a period of 1.25 ns. The sync registers are clocked by the slow clock core_clock0 at 100 MHz, or a period of 10 ns. By default, the Quartus II timing analyzer assumes that data is launched and latched on consecutive active clock edges (Figure 6).

Figure 6. Overly Conservative Timing Estimate



As illustrated in Figure 6, the Quartus II software analyzes the design by taking only 1.25 ns for the data transfer between the output of altlvds and the sync registers. This is overly conservative because the enable pulse guarantees that only one of the high-speed transmitter clock edges are relevant in any given low-speed core clock period. To correct this, you must add a multicycle timing assignment to the Quartus II software, indicating which edges the timing analyzer must use (Figure 7).

Figure 7. Selection of the Proper Launch & Latch Edges



To set up the multicycle value, use the following formula:

set_instance_assignment -name SOURCE_MULTICYCLE
<DESERIALIZATION FACTOR> -from <register name> -to
<register name>

- d. 'Enable Clock Latency' setting should be turned on in the Settings/Timing Requirements & Options/More Settings dialog (Assignments Menu)—for the purpose of using altlvds in the external PLL mode, the clock latency setting must be on. There are two types of clock latency settings:
 - Early Clock Latency
 - Late Clock Latency



Refer to the Quartus II Help for additional information on the clock latency settings and their application.

- 7. In the warning dialog box, click OK.
- 8. On Page 3, in the **What is the number of channels?** list, select or type the desired number of channels (if a number is not listed, you can type the desired number of channels). In this example, enter **4** for the number of serial data channels.

- Refer to the *Stratix II Device Handbook* for channel limitations for your target device size.
 - 9. In the **What is the deserialization factor?** list, select the desired deserialization factor number. In this example, enter a deserialization factor (J factor) of **8**. The deserialization factors available in the list are device-family dependent. Click **Next**. Page 4 is shown.
 - 10. Leave the settings in their default state and click **Next**. Page 5 is shown.
 - 11. On Page 5, click Finish.

The altlvds module is built.

This section describes how to generate the altpll megafunction.

- 1. Start the Quartus II software. On the Tools menu, click **MegaWizard Plug-In Manager**. Page 1 is shown.
- 2. Select **Create a new custom megafunction variation** and click **Next**. Page 2a is shown.
- 3. On page 2a, in the **Installed Plug-Ins** list under **I/O**, select **ALTPLL**. In the **Which device family will you be using?** list, select **Stratix II**. In the **What name do you want for the output file?** field, type the name of the output file. Select the output file type. Click **Next**. Page 3 is shown (Figure 8).

Generating an altpll Megafunction

		_
MegaWizard Plug-In Manager [page 3 of 12]		<u> </u>
📩 ALTPLL		
Version 6.0		About Documentation
1 Parameter 2 Output 3 Simulation 4 Summary	_	
Settings Clocks Library Page		
General/Modes Scan/Lock Bandwidth/55 Clock switch	over >	
	Able to implement in Fast PLL	
altpil		
	General	
Inclk0 inclk0 frequency: 100.000 MHz C0,	Which device family will you be using?	Stratix II 🗸
Operation Mode: Normal/Fast PLL sclkout0	Target this configuration for migration to the HardCopy II de	vice family
Clk Ratio Ph (dg) DC (%) enable0	Which device speed grade will you be using?	Any 🗸
)) (but is the frequency of the indext() incut?	100.00 MHz V
Stratix II	what is the riequency of the inclocko input?	
	Set up PLL in LVDS mode Data rate:	800.000 V Mbps
	PLL type	
	Which PLL type will you be using?	
	Fast PLL	
	O Enhanced PLL	
	Select the PLL type automatically	
	Operation mode	
	How will the PLL outputs be generated?	
	Use the feedback path inside the PLL	
	In Normal Mode	
	O In Source-Synchronous Compensation Mode	
	In Zero Delay Buffer Mode Wah as semanashing	
	Create an roin input for an external feedback (External Fee	dback Mode)
	Which output clock will be compensated for?	c0 💙
-		
	Cancel	Back Next > Einish

Figure 8. MegaWizard Plug-in Manager—ALTPLL, Page 3

- 4. In the Which device family will you be using? list, select Stratix II.
- 5. In the **What is the frequency of the inclock0 input?** list, type **100.00** and select **MHz**.
 - A frequency of 800 MHz for sclkout0 can also be produced for an input frequency of 200 MHz. The sclkout0 frequency is 800 MHz because the required data rate is 800 Mb/s.
- 6. Turn on **Set up PLL in LVDS mode**, and in the **Data rate** list, select **800.00** Mbps.
- 7. Under Which PLL type will you be using?, Fast PLL is automatically selected.
 - When the PLL is set up in the LVDS mode, fast PLL is the only option available.
- 8. Click Next. Page 4 is shown (Figure 9).

MegaWizard Plug-In Manager [page 4 of 12]	
ALTPLL Version 6.0	About Documentation
Parameter Settings 2 Output 3 Simulation 4 Sur Ubrary 9ur Paraget General/Modes Scan/Lock Bandwidth/SS 0	mary e lock.switchover
altpl]_sample_file incli60 Uperation Mole: Nemal/Fart PLL Cok Resio Ph (dg) OC (3) col 1/1 0.00 60.00 Stratix	Able to implement in Fast PLL
	90. Create an iplena' input to selectively enable the PLL III Create an 'areget' input to asynchronously reset the PLL III Create an 'pidena' input to selectively enable the phase/freq. detector
	Lock output Create 'backed' output Enable self-reset on loss of lock Udd 'backed' output low for Udd575 cycles after the PLL initializes
	Advanced PLL Parameters Using these parameters is recommended for advanced users only Create output file(s) using the ' <u>A</u> dvanced PLL parameters Configurations with output clock(s) that use cascade counters are not supported Note: PLL type setting must be explicitly set to either 'Enhanced' or 'Fast' PLL
	Cancel < <u>Back</u> Einish

Figure 9. MegaWizard Plug-in Manager—ALTPLL, Page 4

- 9. Under Dynamic configuration, turn off Create optional inputs for dynamic reconfiguration. Under Optional inputs, turn off all of the options. Under Lock output, turn on Create 'locked' output, and turn off Enable self-reset on loss of lock and Hold 'locked' output low. Under Advanced PLL Parameters, turn off Create output file(s) using the 'Advanced' PLL parameters. Click Next. Page 5 is shown.
- 10. On Page 5, leave the settings in their default state and click **Next**. Page 6 is shown.
- 11. On Page 6, leave the settings in their default state and click **Next**. Page 7 is shown (Figure 10).

MegaWizard Plug-In Manager Enage 7 of 121		
ALTPLL Version 6.0		About Documentation
Parameter 2 Odptat 3 Smddaton 4 Sp Setings 2 Odptat 3 Smddaton 9 parameter Cuto Cut2 Cut3 Altpil_sample_file Pold Pold frequency: 100 000 MPc Operation Med: NormalFart PL Cut Cut3 Sectors S	Core/External Output Clock Able to implement in Fast PLL Use this dock Cook Tap Settings Enter output dock frequency: Enter output dock frequency: Clock gubplication factor Clock glupplication factor Clock glupplication factor Clock glupplication factor Clock glupplication factor Clock dglupplication factor Clock dglupplicati	Epoc Epoce Epoce Requested settings Actual settings 100.0000000 MHz 100.000000 1 Image: Copy 1 22.50 Image: Copy 1 100 Image: Copy 1 22.50 Image: Copy 1 100 Image: Copy 1 22.50 Image: Copy 1 100 Image: Copy 1 20.00 Image: Copy 1 Per Clock Feasibility Indicators CO C1
		Cancel < <u>Back</u> <u>N</u> ext > <u>Einish</u>

Figure 10. MegaWizard Plug-in Manager — ALTPLL, Page 7

- 12. Turn on Use this clock.
- 13. Under Clock Tap Settings, select Enter output clock parameters. For Clock multiplication factor, type 1. For Clock division factor, type 1.
- 14. Turn on **Create sclkout0/enable0 outputs**, and turn on **Enable sclkout phase shift edit**.
- 15. Under Clock Tap Settings, for Clock phase shift, enter -22.50, and select deg. For the Sclkout phase shift, enter -180 and select deg. For Clock duty cycle (%), enter 50.00.
 - The phase shift of the output clock sclkout0 is set to -180 degrees with respect to the VCO clock. The core clock phase shift is set to -22.5 degrees. This is calculated by dividing the sclkout phase shift by the clock multiplication factor of 8, as shown in Equation 1:

(1)

- For more information about the relationship between VCO clock and the PLL output clocks, refer to the *Enhanced PLL Hardware Overview* section in the *PLLs in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II Device Handbook*.
 - 16. Click Next. Page 8 is shown.
 - 17. On Page 8, leave the settings in their default state and click **Next**. Page 9 is shown.
 - 18. On Page 9, leave the settings in their default state and click **Next**. Page 10 is shown.
 - 19. On Page 10, leave the settings in their default state and click **Next**. Page 11 is shown.
 - 20. On Page 11, click Finish.

The altpll module is built.

The advantage of introducing phase shift is to make sure that input data is captured properly as the data appears at the altlvds pin before the rising edge of the sclkout0 as shown in the Figure 11.



Note to Figure 11:

(1) It is assumed that data and clock are edge-aligned. If this is not true, adjust the phase shift.

Simulation

You can use the design file lvds_pll.zip to simulate the design. The lvds_plI.zip file contains the following files:

- Quartus_stratixii_extpll.zip. This file contains the Quartus II project.
- Sim_stratixii_extpll_rtl.zip. This file contains the script files to simulate the gate-level netlist using ModelSim. The gate-level netlist is generated using the Quartus II software, version 5.1, and the simulation models should refer to the Quartus II software, version 5.1. The following three script files are located in the directory:
 - **comp_altera_lib.do**. Use this file to compile the Altera library files for Stratix II components.
 - **comp_gate.do**. Use this file to compile the gate-level netlist and the testbench.
 - **sim.do**. Use this file to load the library and the design to ModelSim, and run the design.

To simulate the RTL netlist using ModelSim, use the script files contained in the following file located in your simulation directory:

- Sim_stratixii_extpll_rtl.zip. This file contains the script files to simulate the RTL netlist using ModelSim.
 - **comp_altera_lib.do**. This file compiles the Altera library files for Stratix II components.
 - **comp_rtl.do**. This file compiles the rtl-level netlist and the testbench.
 - **sim.do**. This file loads the library and the design to ModelSim, and runs the design.

For additional information, refer to the *altlvds Megafunction User Guide*, the *altpll Megafunction User Guide*, and the *PLLs in Stratix II & Stratix II GX Devices* chapter in volume 2 of the *Stratix II Device Handbook*, available on the Altera website: www.altera.com.